

1: About these schematics.
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3: These original MM/1 Schematics represent a valuable resource for the MM/1
4: community. They can also be dangerous.
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6: The CPU board schematics, in particular, do not represent a perfect match to any
7: known board released to the public. The VSC chip used in this set is the
8: 66470B, a development version of the chip which was never widely released. The
9: pinout is DIFFERENT than the final release version, which has 4 pins less. While
10: much of the information IS applicable to version 1.1+ CPU boards, some of it is
11: clearly not. The sound header, for example, is identified as P3 - later used
12: to id the front panel reset button connector. These files are also pretty
13: fuzzy, making them quite difficult to read at times.
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15: Even those parts which can be read, pose hazards. Particularly P13, which
16: forces PIN2 of the floppy drive output high. While this is not a flaw in the
17: diagrams themselves, it is worth noting. This line was used on early drives
18: to manage write compensation as drive heads moved further inward on the
19: platter. On later drives it selected between low and high density. Tying this
20: line high on more modern drives, will melt the cable from the CPU board out.
21: It's an impressive effect, but undesirable.
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23: In short - use of these schematics should be undertaken with caution, and
24: careful attention to as complete a set of secondary sources as possible. The
25: Signetics prerelease and post release documentation for the 66470 are
26: especially necessary.
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29: The version 2.0 I/O board schematic is incomplete. Parts of the diagram fade
30: out at the edge, and only the sound, joystick and serial port /t2 are present.
31: The labels are more legible than the CPU board images.
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33: The version 3.0 I/O board schematics are more complete, and do provide some
34: overlap to the version 2 schematic which is analogous to the MFP/ADC image of
35: this set. This set does not include the memory circuits found on the V2.0
36: board, which remains to some extent "terra incognita". But, they are highly
37: legible.
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39: The SCSI image is notable for its inclusion of hand made markings generated in
40: diagnosing the manufacturing flaw in Version 3 I/O boards which rendered the
41: hard drive and parallel port circuits unusable. This is addressed in the Board
42: Assembly Note image - thanks to Ray Patterson who provided the hands on
43: analysis and implemented the corrections to which Kevin Pease's input pointed.
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46: The set also includes a schematic for ONE paddle board - the MIDI in/out/?thru
47: board. Circuits are definitely available for Midi In and Midi Out, though the
48: DB9 connector used is quite un-standard. It is necessary to remove two jumpers
49: from CPU board P10 jump point, which toggle control lines on the T1 serial port
50: involved.
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52: What's missing from this set (aside from up to date replacements for the CPU
53: board), are schematics for the Mini-bus in both standard and 8-meg expansion
54: forms, serial paddle boards, and the I2C networking paddleboard.
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56: Which would still leave open the question of just what a "non-mini" bus card
57: might look like....
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